# **FPC Manufacturing process**

#### **Material Preparation (Pre-Clean)**

Production panels chemically cleaned, prior to application of circuit forming photo resist film, to ensure proper film. Conveyorized process utilizing thin core handling equipped systems to prevent damage to ultra thin material cores.

#### **Circuit Pattern Exposure**

Photo resist coated panels, overlayed with circuit artwork patterns, exposed with collimated UV light to transfer circuit image(s) to production panels. Both sides exposed simultaneously if required.

#### **Etch Process**

Circuit patterns chemically etched using specialized thin core handling equipped conveyorized systems. Both sides of panels etched simultaneously if required.

#### **Drilling Process**

High speed, high precision, small hole capable, drilling systems create required circuit hole patterns in production panels. Laser based systems available for ultra small hole requirements.

### **Copper Plating Process**

Fully automated electrolytic copper plating systems deposit required additional copper within plated through holes to form layer to layer electrical interconnects.

#### **Coverlay Application**

Polyimide Coverlays aligned and tacked into place on production panels prior to Coverlay lamination process.

## **Coverlay Lamination**

Coverlays laminated to production panels under heat, pressure and vacuum to ensure proper adhesion.

## **Stiffener Application**

Localized additional stiffeners (if required by specific design) aligned and applied prior to additional lamination process under heat, pressure and vacuum.

#### **Electrical Test**

100% netlist driven electrical test per IPC –ET-652. Simultaneous testing of all circuits for continuity and isolation. Both grid and flying probe test systems utilized.

#### **Final Fabrication**

Individual parts die cut from production panel using high precision male / female punch and die sets. Other methods include laser cutting, mechanical routing, steel rule dies and chemically milled dies depending upon specific design requirements.